

REMARKS

The Examiner's Action mailed on January 15, 2008, has been received and its contents carefully considered. A Petition for a Two-month Extension of Time is filed herewith, extending the period for response to June 15, 2008, or to June 16, 2008, being the next working day in the District of Columbia.

In this Amendment, Applicants have amended claims 1-3. Claim 1 is the only independent claim pending and under consideration, and claims 1-4 remain pending and under consideration in the application, claims 5-7 having been withdrawn from consideration. For at least the following reasons, it is submitted that this application is in condition for allowance.

The phrase "electric current blocking portion" in the claims as amended refers to, for example, 10a in FIG. 1B and 10b in FIG. 2, and is a structural portion that is formed between the upper electrode 8 and the exposed surface of the semiconductor lamination portion 6.

The recitation of "the electric current blocking portion preventing electric current from flowing into a part of the semiconductor lamination portion under the upper electrode through the electric current blocking portion "in claim 1 is merely for explaining the operation of the electric current blocking portion.

Claims 1-4 were rejected under 35 USC §112, ¶2 as indefinite, and this rejection is respectfully traversed.

The phrase "and with the light transmitting conductive layer" has been amended to read -- and *to be in contact* with the light transmitting conductive layer *on a periphery of the part removed* --.

Claims 1-2 and 4 were rejected under 35 USC §102(b) as anticipated by, or alternatively under 35 USC §103(a) as obvious solely over, *Kunisato et al.* (US 5,990,496). These rejections are each respectfully traversed.

It is difficult to diffuse current over the entire chip since it is the case with nitride semiconductor light emitting devices that the carrier density of particularly the p-type layer cannot be increased, so a structure is employed in which a light transmitting conductive layer is provided on the surface such that light is extracted from the surface while current is spread over the entire chip, because it is generally desired to extract light from the surface.

The present invention provides solutions for two problems at once, namely that the adhesiveness between the pad electrode (electrode for wire bonding; upper electrode of the present invention) provided on the surface of the light transmitting conductive layer and the transmitting conductive layer is poor, and that the external quantum efficiency is degraded because the upper electrode does not transmit light so that light emitted under the upper electrode cannot be effectively extracted towards the surface side.

Therefore, in the present invention an electric current blocking portion is formed on an exposed surface of the semiconductor lamination portion exposed by removing a part of the light transmitting conductive layer for preventing current

from flowing into the lower side of the upper electrode as much as possible since light emitted upon flow of current to the lower side of the upper electrode cannot be effectively extracted, and in that the upper electrode is formed on the electric current blocking portion, so as to adhere to the semiconductor lamination portion and to be in contact with the light transmitting conductive layer on a periphery of the part removed

Kunisato et al. discloses a semiconductor laser in FIG. 5 thereof, arranged so that the upper electrode is in contact with a p-type GaN contact layer 59 in a stripe-like manner while a current blocking layer 60 is interposed at other portions such that the electrode does not come into contact with the contact layer 59. In other words, since the arrangement of *Kunisato et al.* is a semiconductor laser diode in which light is emitted from a edge face of a part thereof, that is, under the p-electrode 61 rather than being a light emitting diode of which the light is extracted from the surface, and due to this fact, it does not include a light transmitting conductive layer on the surface thereof and it is an element that permits light emission on a lower side of the upper electrode, *Kunisato et al.* is accordingly basically different from the structure of the present invention in which current is diffused over the entire chip by means of the light transmitting conductive layer and in which the electric current blocking portion is interposed so as to prevent current from flowing into the lower side of the upper electrode.

Kunisato et al. accordingly does not include an electric current blocking portion at a contact portion between the upper electrode and the semiconductor lamination portion, or in other words *Kunisato et al.* does not teach or suggest "an electric current blocking portion formed on the exposed surface of the semiconductor lamination portion" where an "upper electrode is adhered to the electric current blocking portion" as recited in claim 1. Instead, *Kunisato et al.* includes a current blocking layer 60 at portions other than the contact portion between the upper electrode and the semiconductor.

The Office Action withholds patentable weight from the following recitation in claim 1 as filed, alleging that it is functional language:

"wherein an electric current blocking means is formed on the exposed surface of the semiconductor lamination portion which is formed by removing a part of the light transmitting conductive layer, thereby preventing electric current from flowing into a part under the upper electrode while ensuring good adhesion between the upper electrode and the surface of the semiconductor lamination portion"

However, this part of claim 1 has now been amended to read as follows:

– an electric current blocking portion formed on the exposed surface of the semiconductor lamination portion, the electric current blocking portion preventing electric current from flowing into a part of the semiconductor lamination portion under the upper electrode through the electric current blocking portion, wherein the upper electrode is adhered to the electric current blocking portion of the surface of the semiconductor lamination portion–

The claim language as amended is not believed to be functional, and thus should be accorded patentable weight.

Accordingly, claim 1 patentably defines over *Kunisato et al.* and is allowable, together with claims 2 and 4 that depend therefrom.

Claim 3 was rejected under 35 USC §103(a) as obvious over the combination of *Kunisato et al.* with *Ota et al.* (US 2003/0001161 A1). This rejection is respectfully traversed.

Claim 3 depends from claim 1, and as *Ota et al.* fails to remedy the deficiencies of *Kunisato et al.* with respect to claim 1, claim 3 is also allowable.

Further, whilst the Office Action alleges that an oxygen containing layer is disclosed in FIG. 1 and ¶[0039] of *Ota et al.* (page 6, line 10 of the Office Action), *Ota et al.* merely recites providing an insulating layer of SiO₂ on the surface, whereas in the present invention oxygen is contained in the nitride semiconductor layer for the purpose of blocking current from flowing.

Claims 1-4 were rejected under 35 USC §103(a) as obvious over the combination of *Chang et al.* (US 6,583,443 B1) with *Shakuda et al.* (US 6,107,644). This rejection is respectfully traversed.

Chang et al. is directed to an AlGaInP-based compound semiconductor light emitting device, and focuses on elimination of a GaAs substrate by adhering a semiconductor laminating portion on a transparent substrate for eliminating losses caused through absorption of light by the GaAs of the substrate, and it is not a nitride semiconductor light emitting device. Further, the structure of FIG. 4C of *Chang et al.* is not arranged such that the upper electrode (metal layer 48B)

contacts a periphery of the part in which the light transmitting conductive layer **44** has been removed. In addition, as described in column 6, lines 15 to 17 of *Chang et al.* "the contact between the metal layer **48B** and the transparent electrode **44** is of Shockley contact", whereas in the present invention electric current blocking between the upper electrode (metal layer **48B** of *Chang et al.*) and the light transmitting conductive layer (transparent electrode **44** of *Chang et al.*) is intended.

Chang et al. therefore also fails to teach or suggest a current blocking portion between the upper electrode and the semiconductor layer, that is to say "an electric current blocking portion formed on the exposed surface of the semiconductor lamination portion" where an "upper electrode is adhered to the electric current blocking portion" as recited in claim 1.

Shakuda et al. is relied upon in the Office Action only for allegedly teaching the internal structure of the semiconductor lamination portion, and so neither *Chang et al.* nor *Shakuda et al.*, whether taken separately or in combination, teach or suggest "an electric current blocking portion formed on the exposed surface of the semiconductor lamination portion" where an "upper electrode is adhered to the electric current blocking portion" as recited in claim 1.

Consequently, claim 1 patentably distinguishes over *Chang et al.* and *Shakuda et al.*, and is allowable, together with claims 2-4 that depend therefrom.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should the remittance be accidentally missing or insufficient, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



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Date

Alun L. Palmer – Registration No. 47,838
RABIN & BERDO, PC – Customer No. 23995
Facsimile: 202-408-0924
Telephone: 202-371-8976

ALP/pq